1. A voltage regulator having an input terminal and an output terminal, comprising:

a printed circuit board;

a substrate mounted on the printed circuit board;

a first flip-chip type integrated circuit chip mounted on the substrate, the first integrated circuit chip including a first power switch fabricated therein to alternately couple and decouple the input terminal to the output terminal;

a filter disposed to provide a substantially DC voltage at the output terminal; and

a control circuit to control the power switch to maintain the DC voltage substantially constant.

2. The voltage regulator of claim 1, wherein the power switch and filter form a buck-converter topology.

3. The voltage regulator of claim 1, wherein the integrated circuit chip is mounted on the substrate with an array of solder bumps or solder balls.

4. The voltage regulator of claim 1, wherein the substrate is mounted on the printed circuit board with solder balls.

5. The voltage regulator of claim 1, wherein the flip-chip type integrated circuit chip includes a p-type region and an n-type region, and the power switch includes a plurality of p+ regions fabricated in the n-type region, and a plurality of n+ regions fabricated in the p-type region, and wherein alternating p+ regions are connected to the input terminal and to an intermediate terminal, and alternating n+ regions chip are connected to the intermediate terminal and to ground.

6. The voltage regulator of claim 1, wherein a portion of the control circuit is fabricated on the first chip.

7. The voltage regulator of claim 1, wherein the portion of control circuit fabricated on the first chip includes a sensor that directs measurements to the portion of the control circuit

fabricated on the second chip.

8. The voltage regulator of claim 1, wherein at least a portion of the control circuit is fabricated in a second integrated circuit chip electrically coupled to the printed circuit board separately from the first chip.

9. The voltage regulator of claim 8, wherein the portion of control circuit fabricated on the first chip includes an interpreter to interpret commands from the portion of the control circuit fabricated on the second chip.

10. The voltage regulator of claim 1, wherein the filter is electrically coupled to the printed circuit board separately from the first chip.

11. The voltage regulator of claim 1, wherein the filter is electrically coupled to the substrate separately from the first chip.

12. The voltage regulator of claim 1, wherein the first power switch intermittently couples an intermediate terminal to the input terminal.

13. The voltage regulator of claim 12, wherein the first flip-chip type integrated circuit chip has a second power switch fabricated therein to alternately couple and decouple the intermediate terminal to ground.

14. The voltage regulator of claim 13, wherein the filter is electrically coupled between the output terminal and the intermediate terminal.

15. The voltage regulator of claim 13, wherein the first power switch includes a distributed array of PMOS transistors and the second power switch includes a distributed array of NMOS transistors.

16. The voltage regulator of claim 12, further comprising a rectifier connecting the

intermediate terminal to ground.

17. The voltage regulator of claim 16, wherein the rectifier is connected to the printed circuit board separately from the first chip.

18. The voltage regulator of claim 1, wherein the filter includes an inductor electrically coupling the first power switch to the output terminal.

19. The voltage regulator of claim 18, wherein the inductor is mounted on the substrate.

20. The voltage regulator of claim 18, wherein the inductor is mounted on the printed circuit board.

21. The voltage regulator of claim 1, wherein the filter includes a capacitor electrically coupling the output terminal to ground.

22. The voltage regulator of claim 21, wherein the capacitor is mounted on the substrate.

23. The voltage regulator of claim 21, wherein the capacitor is mounted on the printed circuit board.

24. The voltage regulator of claim 1, further comprising an input capacitor connecting the input terminal to ground.

25. The voltage regulator of claim 24, wherein the input capacitor is mounted on the substrate.

26. The voltage regulator of claim 24, wherein the input capacitor is mounted on the printed circuit board.

27. An integrated circuit chip with a power switch for a voltage regulator fabricated

thereon, comprising:

a substrate having a first plurality of doped regions and a second plurality of doped regions, the first and second pluralities of doped regions arranged in a first alternating pattern; and

an array of metalized pads fabricated on a surface of the substrate, the array including a first plurality of pads and a second plurality of pads, with the first and second pluralities of pads arranged in a second alternating pattern;

wherein the first plurality of pads are electrically connected to the first plurality of doped regions and the second plurality of pads are electrically connected to the second plurality of doped regions, and wherein the first plurality of pads are connected to a first terminal of the voltage regulator and the second plurality of pads are connected to a second terminal in the voltage regulator.

28. The chip of claim 27, wherein the second alternating pattern is a first set of alternating stripes.

29. The chip of claim 28, wherein the first alternating pattern is a second set of alternating stripes oriented orthogonally to the first set of alternating stripes.

30. The chip of claim 27, wherein the second alternating pattern is a checkerboard pattern.

31. The chip of claim 27, wherein the first and second pluralities of doped regions are p+ regions formed in an n-type well or substrate.

32. The chip of claim 31, wherein the first terminal is an input terminal and the second terminal is an intermediate terminal.

33. The chip of claim 27, wherein the first and second pluralities of doped regions are n+ regions formed in a p-type well or substrate.

34. The chip of claim 33, wherein the first terminal is a ground terminal and the second

terminal is an intermediate terminal.

35. The chip of claim 27, wherein the first plurality of pads are connected to a first plurality of solder balls and the second plurality of pads are connected to a second plurality of solder balls interleaved with the first plurality of solder balls across a surface on the chip.

36. A power switch for a voltage regulator having an input terminal and an output terminal, comprising:

a PMOS switch fabricated on a chip with a first alternating pattern of source pads and drain pads;

an NMOS switch fabricated on the chip with a second alternating pattern of source pads and drain pads; and

a substrate having a first signal layer with a first electrode to electrically couple the drain pads of the PMOS and NMOS switches to an intermediate terminal, a second electrode to electrically couple the source pads of the PMOS switch to the input terminal, a third electrode to electrically couple the source pads of the NMOS switch to ground.

37. The power switch of claim 36, wherein the first and second alternating patterns are alternating rows.

38. The power switch of claim 36, wherein the first and second alternating patterns are checkerboard patterns.

39. The power switch of claim 36, wherein the first electrode has a body and a first plurality of fingers that extend from the body toward the second electrode, the second electrode has a body and plurality of fingers that extend toward the first electrode, the first plurality of fingers are interdigited with the fingers of the second electrode, and each finger overlies and is electrically coupled to a row of pads on the chip.

40. The power switch of claim 39, wherein the first electrode has a second plurality of fingers that extend from the body toward the third electrode, the third electrode has a body

and a plurality of fingers that extend toward the first electrode, the second plurality of fingers are interdigited with the fingers of the third electrode, and each finger overlies and is electrically coupled to a row of pads on the chip.

41. The power switch of claim 36, wherein the substrate includes a second signal layer formed on an opposite side of the substrate from the first signal layer.

42. The power switch of claim 41, further comprising conductive vias through the substrate to electrically connect the first signal layer to the second signal layer.

43. The power switch of claim 36, further comprising solder balls to electrically connect the rows of pads to the first, second and third electrodes of the first signal layer.

44. A power switch for a voltage regulator, comprising:

a chip having an array of pads formed thereon, each pad connected to a plurality of doped regions to create a distributed array of transistors; and

a substrate having a signal layer formed thereon, the signal layer having a first electrode and a second electrode, the first electrode having a body and a plurality of fingers that extend from the body toward the second electrode, the second electrode having a body and plurality of fingers that extend toward the first electrode, wherein the fingers of the first electrode and are interdigited with the fingers of the second electrode and each finger overlies and is electrically coupled to a row of pads on the chip.

45. A voltage regulator having an input terminal and an output terminal, comprising:

a printed circuit board;

a first flip-chip type integrated circuit chip mounted directly on the printed circuit board, the first integrated circuit chip including a first power switch fabricated therein to alternately couple and decouple the input terminal to the output terminal;

a filter disposed to provide a substantially DC voltage at the output terminal; and

a control circuit to control the power switch to maintain the DC voltage substantially constant.